REMARKS

Pending claim 1 calls for defining a multilevel cache including a core have relatively faster components and a region including relatively slower components. A line replacement policy is implemented in said region including relatively slower components.

The office action suggests that Arimilli does not specifically teach that the multilevel cache has a core having faster components and a region having slower components, as recited in the claim. If this is so, then Arimilli does not teach having a core and a region as claimed and, further, cannot teach implementing a line replacement policy in the region. Thus, the pertinency of Arimilli is obscure.

Mohamed is cited as teaching a cache system which includes a cache memory and/or scratch pad wherein the cache is slower than the scratch pad to improve the access time across the address space of a processor. It is further suggested that "since the technology for implementing a multilevel cache system configured with one partition having slower components than the other partition, and since this feature would improve access time as evidenced by Mohamed, an artisan would have been motivated to implement a multilevel cache that has a core having faster components and a region having slower components in the system of Arimilli."

While, certainly, this argument is not accepted, but, if it were accepted for purpose of argument only, it still does not reach the claimed invention. Even if Arimilli were modified to have regions of faster and slower components as postulated in the Examiner's rejection, based on Mohamed, it still does not meet the scope of the claimed invention.

Namely, the scope of the claimed invention further requires implementing the line replacement policy in the region including relatively slower components. Nothing in Mohamed or Arimilli suggests implementing the line replacement policy in a region with slower components.

Moreover, there is really nothing in Mohamed which suggests having a region with slower components. The Examiner's postulated theory is that faster and slower regions could be partitioned, but each of those partitions still has the same components and, therefore, there would not be faster or slower components (even if one region were faster than another for other reasons based on how components of the same speeds are configured).

For at least these reasons, reconsideration of the rejection is respectfully requested.

Respectfully submitted,

Date: February 14, 2005

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation